## CLAIMS

We claim:

1. A method for current calibration of I/O cells of an integrated circuit (IC) comprising:

setting a global control value provided to the I/O cells;

then, for each I/O cell:

comparing the logic voltage at the output pad of the I/O cell with a reference voltage;

sinking more current at the output pad by enabling additional driver bits associated with the I/O cell if the logic voltage is higher than the reference voltage; or

sinking less current at the output pad by disabling additional driver bits associated with the I/O cell if the logic voltage is lower than the reference voltage.

2. The method of claim 1 wherein the sinking of more or less current continues until the logic voltage at the pad and the reference voltage are substantially equal.

3. The method of claim 1, wherein the enabling/disabling of the additional driver bits is accomplished by modifying a local value stored in a register device associated with the I/O cell depending on the comparison of the logic voltage and the reference voltage.

4. The method of claim 3, wherein the local value is modified by shifting 1s or 0s into the register device.

5. The method of claim 1, wherein register device is a counter and the local value is modified by incrementing or decrementing the local value.

6. A method comprising:

setting a global control value provided to the I/O cells;

then, for each I/O cell:

setting a local value in a register device associated with the I/O cell in response to the global control value;

comparing the logic voltage at the output pad of the I/O cell with a reference voltage;

sinking more current at the output pad by enabling additional driver bits associated with the I/O cell if the logic voltage is higher than the reference voltage; or

sinking less current at the output pad by disabling additional driver bits associated with the I/O cell if the logic voltage is lower than the reference voltage.

7. The method of claim 6, wherein the enabling of the additional driver bits comprises modifying the local value in the register device associated with the I/O cell in response to the comparison of the logic voltage and the reference voltage.

8. The method of claim 6, wherein the disabling of the additional driver bits comprises modifying the local value in the register device associated with the I/O cell in response to the comparison of the logic voltage and the reference voltage.